Amendments to the Claims:

This listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1(currently amended):

A processing method for forming silicide comprising:

providing a semiconductor structure having a semiconductor surface and an insulation surface;

forming an epitaxial layer on said semiconductor surface together with residues of said epitaxial layer on said insulation surface;

treating said semiconductor structure, wherein said treating step is that a removal rate of ~~said residues of said epitaxial layer on~~ said insulation surface on which has said residues of said epitaxial layer is higher than a removal rate of said epitaxial layer on said semiconductor surface to remove said residues of said epitaxial layer together with a portion of said insulation surface;

forming a metal layer on said epitaxial layer; and

heating said epitaxial layer for forming silicide.

Claim 2(original):

The processing method according to claim 1, wherein providing said semiconductor structure step comprises forming a substrate and forming a gate electrode for forming a portion of said semiconductor structure.

Claim 3(original):

The processing method according to claim 2, wherein forming said semiconductor surface step comprises forming a doped region in said substrate for forming a portion of said semiconductor surface.

Claim 4(original):

The processing method according to claim 2, wherein forming said semiconductor surface step comprises forming an upper surface on said gate electrode for forming a portion of said semiconductor surface.

Claim 5(original):

The processing method according to claim 2, wherein forming said insulation surface step comprises forming a spacer on the sidewall of said gate electrode for forming a portion of said insulation surface.

Claim 6(original):

The processing method according to claim 2, wherein forming said insulation surface step comprises forming an insulation device in said substrate for forming a portion of said insulation surface.

Claim 7(original):

The processing method according to claim 1, wherein forming said epitaxial layer comprises forming epitaxial silicon.

Claim 8(original):

The processing method according to claim 1, wherein forming said epitaxial layer comprises forming an epitaxial silicon compound.

Claim 9(original):

The processing method according to claim 1, wherein said treating step comprises executing wet etching for removing a portion of said insulation surface.

Claim 10(original):

The processing method according to claim 9, wherein said wet etching comprises using fluorine-containing solution.

Claim 11(original):

The processing method according to claim 1, wherein said treating step comprises executing dry etching for removing a portion of said insulation surface.

Claim 12(original):

The processing method according to claim 11, wherein said dry etching comprises using a fluorine-containing compound.

Claim 13(original):

The processing method according to claim 1, wherein forming said metal layer comprises forming a titanium (Ti) layer.

Claim 14(original):

The processing method according to claim 1, wherein forming said metal layer comprises forming a cobalt (Co) layer.

Claim 15(currently amended):

A processing method for forming silicide comprises:

providing a silicon substrate;

forming a polysilicon gate electrode on said silicon substrate;

forming an insulation spacer on a sidewall of said polysilicon gate electrode;

forming an epitaxial layer on said silicon substrate and an upper surface of said polysilicon gate electrode together with residues of said epitaxial layer on said insulation spacer;

etching said residues of said epitaxial layer, epitaxial layer and a portion of said insulation spacer, wherein a removal rate of ~~said residues of said epitaxial layer on~~ said insulation spacer on which has said residues of said epitaxial layer is higher than a removal rate of said epitaxial layer on said silicon substrate and said upper surface of said polysilicon gate electrode to remove said residues of said epitaxial layer together with said portion of said insulation spacer;

forming a metal layer on said epitaxial layer; and

heating said epitaxial layer for performing salicidation on said upper surface of said polysilicon gate electrode and said silicon substrate.

Claim 16(original):

The processing method according to claim 15, wherein said etching step comprises executing wet etching with fluorine-containing solution.

Claim 17(original):

The processing method according to claim 15, wherein said etching step comprises executing dry etching with fluorine-containing compound.